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(54) **CHANGING OVER METHOD FOR DOUBLED ATM SWITCH SYSTEM.**

(57) A system changing over method for a cell exchange system, which has doubled asynchronous transfer mode (ATM) switches for exchanging ATM cells, and can change over the ATM switches correctly without the lack and duplication etc. of the cells. On the input sides of the ATM switches, bits which show being active for the switch of an active system and being stand-by for the switch of a stand-by system respectively are inserted into the headers of the cells sent from a transmission line respectively and are inputted to the ATM switches; on the output sides of the ATM switches, corresponding bits in the headers of the cells outputted from the respective switches of the doubled ATM switch are referred to, only cells which show being active are selected and are outputted to the transmission line. On the output sides of the respective ATM switches, buffers for storing the cells which show being active are provided respectively. When changing over the system, inputting cells into the previous active system is stopped and the cells which show being active are stored in the new active system. After all the cells which show being active in the previous active system are outputted, the cells which show being active stored in the buffer of the new active system are outputted.

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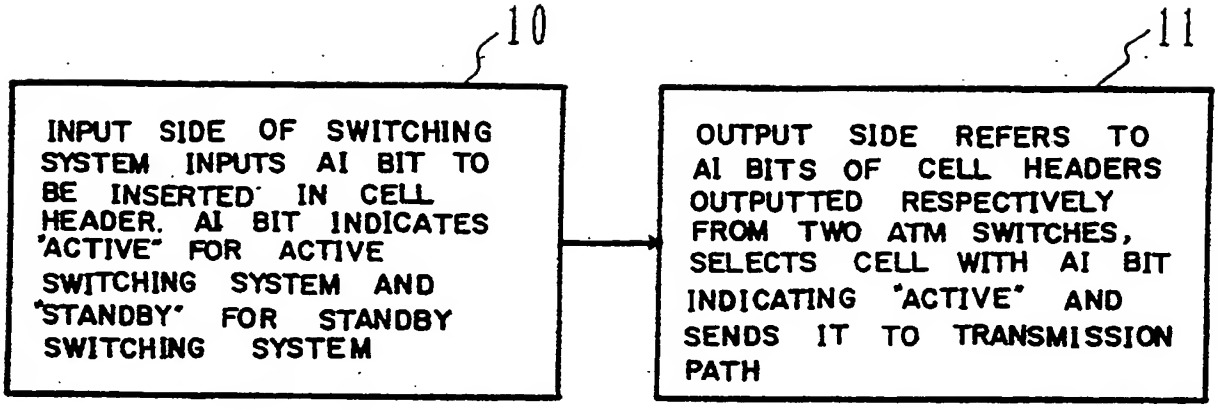
10
INPUT SIDE OF SWITCHING SYSTEM INPUTS AI BIT TO BE INSERTED IN CELL HEADER. AI BIT INDICATES "ACTIVE" FOR ACTIVE SWITCHING SYSTEM AND "STANDBY" FOR STANDBY SWITCHING SYSTEM
11
OUTPUT SIDE REFERS TO AI BITS OF CELL HEADERS OUTPUTTED RESPECTIVELY FROM TWO ATM SWITCHES, SELECTS CELL WITH AI BIT INDICATING "ACTIVE" AND SENDS IT TO TRANSMISSION PATH

Fig. 5

Field of the Invention

The present invention relates to a system for switching between systems in an exchange system in which an ATM switch is duplexed.

Background of the Invention

An ATM (Asynchronous Transfer Mode) network, unlike a conventional STM (Synchronous Transfer Mode) network, exchanges and transmits information with information to be transmitted being entered into an information element of a given length which is referred to as a cell. The cell, as shown in Figure 1, is composed of a header for identifying a virtual channel and information containing actual information.

The ATM switch performs routing within the switch on the basis of the contents of the header. Thus, the transfer time of a cell varies with the route. In a duplexed ATM switch as well, the transfer time of a cell varies with its internal state even if the same route is set.

Figure 2 illustrates the system configuration of a conventional duplexed system. ATM data from a transmission line 1 is entered into a transmission line interface 2. The transmission line interface 2 distributes signals to duplexed ATM switches 3 and 4 equally. In both of the duplexed ATM switches 3 and 4, the same routing is performed.

A transmission line interface 5 on the output side receives cells from one of the ATM switches 3 and 4 that is in the active state and sends out them onto a transmission line 6.

Figure 3 illustrates an example of an arrangement of the ATM switch (n x m cross switch). In this Figure, the ATM switch is adapted to output a cell from one of n input highways to one of m output highways.

In Figure 3, the ATM switch is comprised of buffers 7 each of which is placed at an individual one of intersections of the input highways and the output highways, multiplexing sections 8 and highway sources 9 each corresponding to a respective individual output highway. Each of the highway sources 9 is adapted to output a bit indicating whether or not data is present on a corresponding channel, and each of the multiplexers 8 is adapted to capture an empty channel and insert a cell to be switched into the channel.

Figure 4 illustrates a conventional duplexed system in which ATM switches are connected in multistages. In the Figure, ATM switches (cross switches) are connected in three stages. One of outputs of both of the multistage-connected switches is selected by a system selector and then output onto a transmission line.

With the duplexed system using ATM switches shown in Figure 2, however, since the transfer times of cells differ from each other even if the same route is set in the ATM switches 3 and 4, if the receiving-side transmission line interface 5 makes system switching by means of selection of cells, drop-out of cells and overlap between cells will occur. Thus, there is a disadvantage that systems cannot be switched without affecting call processing.

As described in connection with Figure 3, there are provided buffers 7 for contention control in the ATM switch. If, for example, the power supply of one of the systems is turned off for maintenance and turned on again at the termination of the maintenance, a difference will arise between this system and the other system which has continued its operation in respect of data storing states of the buffers in the switches. Thus, there is a problem that drop-out, overlap and overstripping of cells occur if the systems are switched as they are.

Disclosure of the Invention

In view of the above problems of the prior art, it is the object of the present invention to provide a switching system for an ATM switch duplexed system which allows accurate switching to be made between ATM switches so that drop-out of cells and overlap between cells will not occur.

Figure 5 is a functional block diagram of a first system switching system. The figure is a functional block diagram of a first system switching system adapted to insert into an ATM cell a bit indicating that a system is active or on standby and enter it into an exchange.

In Figure 5, at the input side of the exchange, in block 10, an AI bit indicating that the system is active is inserted into the header of a cell from transmission path to the switch in the active system and a bit indicating that the system is on standby is inserted into a cell to the switch in the standby system and entered into the exchange. At the output side of the exchange, in block 11, by referring to the AI bit in the header of each cell output from each of two ATM switches, cells each indicating that its AI bit is active are selected and sent out onto a transmission path.

In the first switching system, there are provided two buffers, each of which stores a cell output from a corresponding one of ATM switches, between the ATM switches and a selector for selecting a cell and outputting it to a transmission path. At the time of switching between the active system and the standby system, entry of cells into the ATM switch of a system which was active is stopped, and only cells indicative of being active are stored in the buffer at the output side of the ATM switch of the system which was on standby. At a point of time

when cells indicative of being active disappear from the buffers within the ATM switch of the system which was active and the buffer at the output side of the ATM switch, the selector starts to output cells from the buffer of the system which was on standby, thereby allowing the ATM switches to be accurately switched without causing drop-out of cells and overlap between cells.

Figure 6 is a block diagram illustrating the principle of a second system switching system. This figure is a block diagram illustrating the principle of a second system switching system for switching between systems without providing an ATM cell with a bit indicating that a system is either active or on standby.

In Figure 6, two cell storage means 12 and 13 are, for example, buffers for storing input ATM cells and provided at the input sides from a transmission line to two ATM switches 14 and 15. A system selecting means 16 is adapted to select either of outputs of the two ATM switches 14 and 15 and output it to a transmission line.

In Figure 6, at the time of switching between systems, outputting of cells from the cell storage means 12 and 13, e.g., buffers, to corresponding ATM switches 14 and 15, is stopped and input ATM cells are stored in the buffers. When residual cells disappear from the ATM switches, the stop applied to outputting of cells from the buffers is canceled and the system selecting means is switched. That the ATM switches have no residual cells can be decided by detecting that the buffers provided at intersections of the input highways and the output highways, which were described in connection with Figure 3, are all vacated.

Brief Description of the Drawings

Figure 1 is a diagram illustrating an arrangement of an ATM switch;

Figure 2 is a diagram illustrating a system configuration of a conventional ATM switch duplexed system;

Figure 3 is a block diagram illustrating an example of an arrangement of an n x m cross switch;

Figure 4 illustrates a conventional duplexed system in which the cross switches are connected in multistages;

Figure 5 is a functional block diagram of a first switching system;

Figure 6 is a block diagram illustrating the principle of a second switching system;

Figure 7 is a diagram illustrating an embodiment of a position into which an active/standby indicating bit is inserted;

Figure 8 is a block diagram illustrating an arrangement of an input-side transmission-line interface in a first embodiment of the ATM switch duplexed system;

Figure 9 is a diagram illustrating an embodiment of ACT controller generating information;

Figure 10 is a block diagram illustrating an arrangement of an output-side transmission-line interface in the first embodiment;

Figure 11 is a diagram illustrating the control of the selector by the selector controller;

Figure 12 is a timing chart of an exemplary operation at the time of switching between systems in the first embodiment;

Figure 13 is a block diagram illustrating a second embodiment of the ATM switch duplexed system;

Figure 14 is a diagram for explaining the switching operation in the second embodiment;

Figure 15 is a timing chart of the system switching process in the second embodiment;

Figure 16 is a flowchart of the system switching process in the second embodiment;

Figure 17 is a diagram illustrating the position of the central processing unit of the exchange system in the second embodiment;

Figure 18 is a diagram illustrating select states of the selector in the second embodiment;

Figure 19 is a block diagram illustrating a third embodiment of the ATM switch duplexed system; and

Figure 20 is a block diagram illustrating a fourth embodiment of the ATM switch duplexed system.

Best Mode for Practicing the Present Invention

The present invention will be described in more detail with reference to the accompanying drawings.

Figure 7 illustrates an embodiment designating a position into which an active/standby indicating bit, which is assigned to the header part of an ATM cell, is inserted in order to indicate that the system is active or on standby. In the figure, an ACT flag serving as the active/standby indicating bit is inserted into a free area of TAG information, which is generally assigned to the header part of a cell at the time of entry into an exchange for exchange control in the exchange, for example, bit position 0. Bit 0 = 1 indicates active, while bit 0 = 0 indicates standby. In the TAG information are stored an output highway number for each of the cross switches connected in, for example, three stages as indicated in Figure 4, and a highway number for a demultiplexer for outputting a cell onto one of plural transmission lines, which is not shown in Figure 4.

Figure 8 is a block diagram of a transmission line interface at the cell input side in a first embodiment of the ATM switch duplexed system. Like

reference numerals, are used to designate corresponding parts to those in Figure 2. In the figure, 160 designates the input transmission line interface section. Reference numeral 17 designates an AI bit inverter which receives cell data and inserts a bit (AI bit) indicative of being active into the header of a cell to be entered in the active system and a bit indicative of being on standby into a cell to be entered into the standby system, and 18 designates an ACT controller which is responsive to information from duplexed ATM switches 3 and 4 to control the operation of the AI bit inserter 17. The AI bit inserter 17 and the ACT controller 18 are contained in the input transmission line interface section 160. The operation of the circuit constructed in this way will be explained as follows.

The ATM switches 3 and 4 constituting the duplexed system can assume either the active (ACT) mode or the standby (SBY) mode. Mode information of the ATM switches 3 and 4 is applied to the ACT controller 18. The ACT controller 18 is responsive to the mode information to generate such information as shown in Figure 9.

That is, when the #0 ATM switch 3 is ACT and the #1 ATM switch 4 is ACT, such information as to retain the previous state is generated. When the #0 ATM switch 3 is ACT and the #1 ATM switch 4 is SBY, such information as renders #0 ACT and #1 SBY is generated. When the #0 ATM switch 3 is SBY and the #1 ATM switch 4 is ACT, such information as renders #0 SBY and #1 ACT. When the #0 ATM switch 3 is SBY and the #1 ATM switch 4 is SBY, such information as to retain the previous state is generated. Such information is applied to the AI bit inserter 17.

When, for example, the ATM switches #0, #1 are both ACT or SBY (such a state can occur at the time of switching between systems), the AI bit inserter 17 inserts into a cell an AI bit of the state it had before both of the switches became ACT. For example, when #0 is ACT and #1 is SBY, the AI bit inserter inserts an AI bit of ACT into a cell to the #0 switch and an AI bit of SBY into a cell to the #1 switch. When the #0 switch is ACT and the #1 switch is SBY, the bit inserter inserts an AI bit of ACT into a cell to the #0 switch and an AI bit of SBY into a cell to the #1 switch. The cells in which AI bits are inserted into their respective headers in this way are applied to the corresponding respective ATM switches 3 and 4 and the switching operation through the same route is performed.

Figure 10 is a block diagram of a transmission line interface at the cell outputting side in the first embodiment of the ATM switch duplexed system. In the figure, 19 designates a buffer for receiving #0 cell data, 20 designates a buffer controller which refers to the AI bit contained in a #1 cell and writes the cell data into the buffer 19 only when the AI bit is ACT, 21 designates a buffer for receiving #1 cell data, and 22 designates a buffer controller which refers to the AI bit contained in a #1 cell and writes the cell data into the buffer 21 only when the AI bit is ACT.

Reference numeral 23 designates a selector for selectively outputting one of outputs of the #0 buffer 19 and the #1 buffer 21 and 24 designates a selector controller which is responsive to output information (information for monitoring the presence or absence of data in the buffers 19 and 21) from the #0 buffer controller 20 and the #1 buffer controller 22 to perform select control of the selector 23. The operation of the circuit thus constructed will be described as follows.

The #0 and #1 buffer controllers 20 and 22 receive their respective cell data to refer to the AI bits inserted into their headers and write cell data transmitted only when the AI bits are ACT into their corresponding respective buffers 19 and 21. The buffer controllers 20 and 22 monitor the states of their respective buffers 19 and 21 to send to the selector controller 24 information about the presence or absence (empty) of data in the buffers 19 and 21. The selector controller 24 is responsive to the information about the states of the buffers 19 and 21 from the systems to control the selector 23 as indicated in Figure 11.

That is, when both of the buffers #0 and #1 are empty or have data, the selector 23 is kept in the previous state. For example, if the buffer #0 has been selected, its selected state is kept as it is. On the other hand, when either of the buffers #0 and #1 has data, the buffer with data is selected.

Next, the operation at the time of switching between systems will be described. At the time of switching between systems, on the input side, after the ACT/SBY for both systems have become stabilized, that is, after the #1 became ACT in Figure 12(c) after the #0 became SBY in Figure 12(b), the AI bit of ACT is inserted into the header of each of cells only for the system which has become ACT anew. On the output side, on the other hand, only cells whose AI bits are ACT are written into the buffers 19 and 21. For this reason, although cells whose AI bits are ACT and cells whose AI bits are SBY are transmitted mixed because of different internal states in the duplexed system, all the AI bits will eventually become SBY and the buffer will become empty in the new SBY system.

In the new ACT system, on the other hand, although cells whose AI bits are SBY and cells whose AI bits are ACT are mixed, all the AI bits will eventually become ACT. When the buffer of the new SBY system becomes empty, data is read from the buffer 19 or 21 under the control of the selector controller 24.

Figure 12 is a timing chart of the operation at

the time of switching between systems. It is assumed that data is entered as indicated in (a) (in the figure blanks indicate vacancy of data). It is assumed here that the ACT/SBY of the #0 and #1 systems is set as indicated in (b) and (c). The AI bits are inserted into the headers of cells according to the ACT/SBY states indicated in (b) and (c). As a result, the ACT, SBY states of #0 data and #1 data will become as shown in (d) and (e) in the figure. Here, A indicated in data Q represents ACT, while S represents SBY.

Since, in the initial state, the #0 system is ACT (hereinafter indicated as A) and the #1 system is SBY (hereinafter indicated as S), #0 data becomes A and #1 data becomes S during this state. At the time of switching between systems (the timing of data Qn + 5), the #0 system is in ACT and the #1 system is in SBY because the previous state is held.

Next, the operation of the output side will be described. In the process in the duplexed ATM switches, the #0 data arrive after a delay of six cells as indicated in (f), while the #1 data arrive after a delay of three cells as indicated in (g) because of different internal states.

Here, if arriving data indicated in (f) and (g) are selected by the use of the #0 and #1 ACT information irrespective of AI bits, the result will become as shown in (h). As is evident from the figure, data Qn + 2 and Qn + 3 are dropped out. The use of the buffer configured as shown in Figure 10 in the output-side transmission line interface section allows only cells whose AI bits are ACT to be written into the buffers as indicated in (i) and (j).

For example, only data of ACT are written into the #0 buffer 19 as indicated in (i). On the other hand, into the #1 buffer 21 as well are written only data of ACT as indicated in (j). As to the #1 buffer, since the first ACT data is Qn + 6, Qn + 6 and following data are written into. Reading of data written into the buffers in this way is performed by the selector controller 24. In this case, reading of the data from the #1 buffer 21 is not performed until the #0 buffer 19 has become vacated. That is, the selector controller 24 selects the #0 buffer 19 until the #0 buffer 19 has been vacated, in other words, until the last data Qn + 5 has been read. Note that it is assumed here that the #1 buffer is read after active cells of buffers placed at intersections in the ATM switch, i.e., n x m cross switch have disappeared.

As a result, the contents of the #0 buffer 19 up to the data Qn + 5 are output from the selector 23 as indicated in (k). It is not until the #0 buffer 19 has been vacated that the selector controller 24 switches the selector 23 to select the #1 buffer 21, so that the contents Qn + 6, Qn + 7 of the #1 buffer 21 are output from the selector 23. In this way, as indicated in (k), successive data are read at the time of switching between systems without causing drop-out of data cells and overlap between cells.

Figure 13 is a block diagram of a second embodiment of the ATM switch duplexed system. In the figure, the system is constructed from an ACT mark assigner section 25 for setting an ACT flag indicating active to the header part of an ATM cell to be input from the input transmission line to the active system of the duplexed system and an ACT flag indicating standby to an ATM cell to be input to the ATM switch of the standby system of the duplexed system, a multiplexer section 26 for regulating, for example, a difference in cell transfer rate between the transmission line and the ATM switch as will be described later, a switch section 27, a demultiplexer section 28 for regulating the cell transfer rate as the multiplexer section 26 does, and a selector section 29 for selecting either of outputs of the duplexed ATM switches.

The ACT mark assigner section 25 assigns ACT flags to ATM cells input from the input transmission line in such a way that the "1" flag is set to cells to be input to the active switch in the switch section 27 and the "0" flag is set to cells to be input to the standby switch. Cells which passed through the ATM switches are checked for their ACT flags with the result that only cells to which the one ACT flag has been set are output to the output transmission line via the demultiplexer section 28 and the selector section 29. Thereby, overlap and drop-out of cells can be avoided.

If, in Figure 13, cells were output in the order in which they were output from the switch section 27, outstripping of cells and so on would occur at the time of switching between systems because of different conditions of buffers in the switch. For this reason, at the time of switching between systems, the input of cells to the old active system is stopped temporarily and the selector section 29 outputs cells from the old active system until all the active indicating cells have passed through the old active system and then the buffers in the switch and the buffers in the demultiplexer section 28 have been vacated. During this period active indicating cells are stored in the buffers of the demultiplexer 28 for the new active system. When all the buffers for the old active system are vacated, the selector section 29 is switched to start to read from the buffers in the demultiplexer section 28 of the new active system. And inputting of ATM cells from the input transmission line to the old active system is resumed.

In Figure 13, the ACT flag assignment is performed by the ACT mark assigner 25 in a simplexing section which is not duplexed. If the ACT flags were assigned in a duplexing section, there would

be the possibility of occurrence of overlap or drop-out of cells in the event of a failure of the flag assignment circuit. At the time of switching between systems, active indicating cells may flow into the switches of both systems, so that even the contents of active cells of both systems are required to be checked and verification of the failure becomes difficult. If the flags are assigned in the simplexing section, it becomes impossible to switch between systems in the event of a failure in the flag assignment circuit. However, the failure can be verified in the succeeding duplexing section. Therefore, the ACT flags are assigned in the simplexing section and they are checked in the duplexing section.

In Figure 13, the selection of active indicating cells can also be carried out by the cell selector using, for example, TAG information. Standby cells can be discarded there. Only active indicating cells are input to the buffers of the demultiplexer section 28 for regulating the rate of transmission of cells of both systems. The rate-regulating buffer is also used as a buffer for avoiding outstripping of cells and provided in the duplexing section.

Figure 14 illustrates the operation at the time of switching between systems in the second embodiment. A description will be made of the operation when the upper system in the second embodiment of Figure 13 is switched from active to standby and the lower system is switched from standby to active. First, in Figure 14(a), inputting of ATM cells to the upper system as old active system and ACT flags are set to input cells by the ACT mark assigner 25 for application to the lower system. Thereby, an active indicating cell with a black square mark is input to the lower system and the buffer in the demultiplexer 28 for the lower system is reset, so that it is placed in the state to store only active indicating cells.

Figures 14(b) and (c) illustrate the operation when switching between systems is being made. In Figure 14 (b), an active indicating cell still remains in the buffer of the demultiplexer 28 of the upper system which is the old active system and the selector 29 outputs the cell from the old active system onto the transmission line. In Figure 14(c), the active cell in the upper system has disappeared and an active indicating cell has been stored in the buffer in the demultiplexer 28 of the lower system which is a new active system.

In Figure 14(d), an ATM cell is output from the buffer of the demultiplexer 28 of the new active system onto the output transmission line via the selector 29. At the same time, inputting of ATM cells to which the "0" ACT flag is set to the old active system, i.e., the standby system is resumed. The reason why cells are input to the standby system as well after system switching is to make the systems equal to each other with respect to the extent of congestion of cells at the time of switching between systems and to allow a check of the route in the standby at the time of standby. In Figure 14, the multiplexer 26 serves to transmit a plurality of low-speed signals from the simplexer simultaneously to the switch section 27, while the demultiplexer 28 serves to convert a high-speed signal from the switch section to low-speed signals to the simplexer.

Figure 15 is a timing chart of the system switching process in the second embodiment. When a system switching instruction is input from the central processing unit (CPU) of the exchange system, switching of assignment of the ACT flag is made first by the ACT mark assigner, inputting of cells to the old active system is stopped, resetting of the buffers in the demultiplexer in the new active system is performed, and storing of only active indicating cells in the buffers is started. Subsequently, a check is made as to whether or not the buffers of the old active system have been vacated. The selector is switched after they have been vacated.

Figure 16 is a flowchart of the system switching process in the second embodiment. In the figure, the presence or absence of a system switching instruction from the CPU is monitored in step S30, and when the instruction is present, in S31, switching of ACT flag assignment is performed, inputting of cells to the old active system is stopped, resetting of the buffers in the new active system is performed, and storage of active cells in the new active system is started. A decision is made in S32 as to whether or not the buffers in the old active system have been vacated. After they have been vacated, in S33, the selector is switched, stoppage of inputting of cells to the old active system is canceled, and storage of active cells in the demultiplexer in the new active system is canceled. The system switching is completed in S34.

Figure 17 illustrates the location of the central processing unit (CPU) of the exchange system in the second embodiment. The CPU 35, as shown, sends #0-system side (upper side) active signals and #1-system side (lower side) active signals to the simplexer via the duplexer.

Figure 18 illustrates select states of the selector which correspond to active signals from the CPU 35. In the figure, when both the 0-system and 1-system are active or standby, the select state prior to change is held. When one of the systems is active and the other is standby, ATM cells from the active system are selected and output.

In connection with Figures 13 through 16, a description was made that the selector 29 is switched when the buffers in the ATM switch in the

old active system and the buffers in the demultiplexer 28 are all vacated. For each of the buffers it is calculated from a count value of a write/read counter how far cells fill and it is decided that the buffers are vacated when the amount of use of buffers is zero. The conditions under which the buffers are vacant are detected for each of switch stages and its information is transmitted to the next switch stage like highway information. The next switch stage computes the AND of its buffer vacancy conditions with the buffer vacancy conditions of the preceding stage. If the buffers in both stages are vacant, the vacancy information of the next stage is likewise transmitted. The demultiplexer 28 computes the AND of the vacancy information received together with the highway information with the buffer vacancy conditions of the buffers in the demultiplexer 28 and performs the operation of switching between systems if all the buffers are vacant.

Figure 19 is a block diagram of a third embodiment of the ATM switch duplexed system. In the figure, buffers 40 and 41 are provided ahead of ATM switches (n x m cross switches) 42 and 43, respectively. Also, switches 44 and 45 are provided between the buffer 40 and the ATM switch 42 and between the buffer 41 and the ATM switch 43, respectively. Either of outputs of the ATM switches 42 and 43 is selected by a system selector 46 for transmission to a transmission line.

In Figure 19, the buffers 40 and 41 have the same depth as the ATM switches 42 and 43, and cells are normally input to the cross switches as they are without being stored in the buffers. However, the switches 44 and 45 are opened in switching between the systems and thus outputting of cells from the buffers is stopped, so that input ATM cells are stored in their respective buffers 40 and 41. On the other hand, cells continue to move inside the cross switches and residual cells eventually disappear from the cross switches. At this point of time the system selector 46 is switched to switch between systems and the switches 44 and 45 are closed to cancel the stoppage of cell outputs from the buffers 40 and 41. Thereby, the switching between system can be carried out with drop-out, overlap and overstripping of cells avoided.

Figure 20 is a block diagram of a fourth embodiment of the ATM switch duplexed system. In the figure, in each system a plurality of, three herein, cross switches are provided, and buffers which correspond in number to the cross switches are connected in series ahead of the cross switches. That is, three buffers are connected in series because the buffer depth on the cross-switch side is tripled. The operation of this embodiment is the same as that of the third embodiment of Figure 19.

The Possibility of Utilizing the Invention in the Industrial View

As described above, the system switching system of the present invention is useful for an exchange system where the ATM switch is duplexed. Also, the present invention is naturally applicable not only to an ATM exchange but also to a general packet exchange.

Claims

1. In an exchange system in which an ATM switch is duplexed, a switching system in an ATM switch duplexed system characterized by:

   at the input side of the exchange system, inserting into the header of each of cells from a transmission line an AI bit indicating being active for an ATM switch in an active system or an AI bit indicating being on standby for an ATM switch in a standby system; and

   at the output side of the exchange system, referring to AI bits of the headers of cells output from the two ATM switches and selecting cells each having the AI bit indicating being active for transmission to a transmission line.

2. A switching system of an ATM switch duplexed system according to claim 1, characterized in that an input transmission line interface provided between the input side of the exchange system and the transmission line is provided with an AI bit inserter for inserting into the header of each of cells input from the transmission line the AI bit indicating being active for the active switch of the two ATM switches or the AI bit indicating being on standby for the standby switch and sending AI-bit inserted cells to corresponding respective switches; and

   an ACT controller connected to receive active/standby indicating signals from the two ATM switches for outputting AI-bit generation information to the AI bit inserter.

3. A switching system of an ATM switch duplexed system according to claim 2, characterized in that the said generation information output from the ACT controller instructs the said AI bit inserter to hold the previous state when the two ATM switches are both active or standing by and instructs the said AI bit inserter to generate an AI bit corresponding to the states of the two ATM switches when one of the two ATM switches is active and the other is standing by.

4. A switching system of an ATM switch duplexed system according to claim 1, characterized in that an output transmission line interface provided between the output of the exchange system and the transmission line is provided with

two buffers for storing ATM cells output from the two ATM switches and having AI bits inserted indicating active;

two buffer controllers for controlling inputting of cells to the two buffers and monitoring the presence or absence of data in the corresponding buffers;

a selector for selecting either of outputs of the two buffers and outputting it to the transmission line; and

a selector controller responsive to monitor outputs of the two buffer controllers for controlling cell output from the selector.

5. A switching system of an ATM switch duplexed system according to claim 4, characterized in that, at the time of outputting of cells from the selector to the transmission line, the selector controller controls the selector in such a way that it maintains the previous cell output state when the two buffers are both vacated or in the state in which data is present or it selects the buffer having data when one of the two buffers is vacated and the other has data.

6. A switching system of an ATM switch duplexed system according to claim 1, characterized in that there is provided an ACT mark assigner, at the input side of the ATM switch duplexed exchange system, for assigning to the header of a cell a bit indicating active for a switch in the active system and indicating standing by for a switch in the standby system for outputting to the ATM switches;

two buffers, at the output side of the two ATM switches, for storing ATM cells output from the switches and assigned active indicating bits; and

a selector for selecting either of the outputs of the two buffers and outputting it to the transmission line.

7. A switching system of an ATM switch duplexed system according to claim 6, characterized in that the selector, provided at the output side of the exchange system, at the time of selecting outputs of the two buffers, maintains the previous select state when the two ATM switches are both active or standing by and, when one of the two ATM switches is active and the other is standing by, selects the output of the buffer on the side of the ATM switch which is active.

8. A switching system of an ATM switch duplexed system according to claim 6, characterized by, in response to a system switching instruction from a central processing unit of the exchange system, switching by the ACT mark assigner the active/standby indicating bit assignment,

stopping inputting cells to the ATM switch of the old active system, resetting the buffer at the output side of the ATM switch of the new active system, then storing only active indicating cells in the buffer and waiting for the buffer in the old active system to be vacated; and

switching the selector when the buffer is vacated and resuming cell input to the ATM switch in the old active system to thereby complete the system switching.

9. A switching system of an ATM switch duplexed system according to claim 1 or 6, characterized by inserting into a vacated area of TAG information, for controlling the exchange of cells in the ATM switch, a 1 when being active or a 0 when standing by as the AI bit or the active/standby indicating bit.

10. In an exchange system in which an ATM switch is duplexed, a switching system in an ATM switch duplexed system characterized by comprising: two cell storage units, respectively provided at inputs side of two ATM switches, for storing input ATM cells; and system selector means, provided at the output side of the two ATM switches, for selecting either of the outputs of the two switches and outputting it to a transmission line, to thereby, at the time of switching between systems, stop outputting of cells from the two cell storage units to corresponding respective ATM switches to store input ATM cells into the cell storage units and cancel the stoppage of outputting of cells and switch the system selector means when residual cells disappear from the ATM switches.

HEADER
INFORMATION

Fig. 1

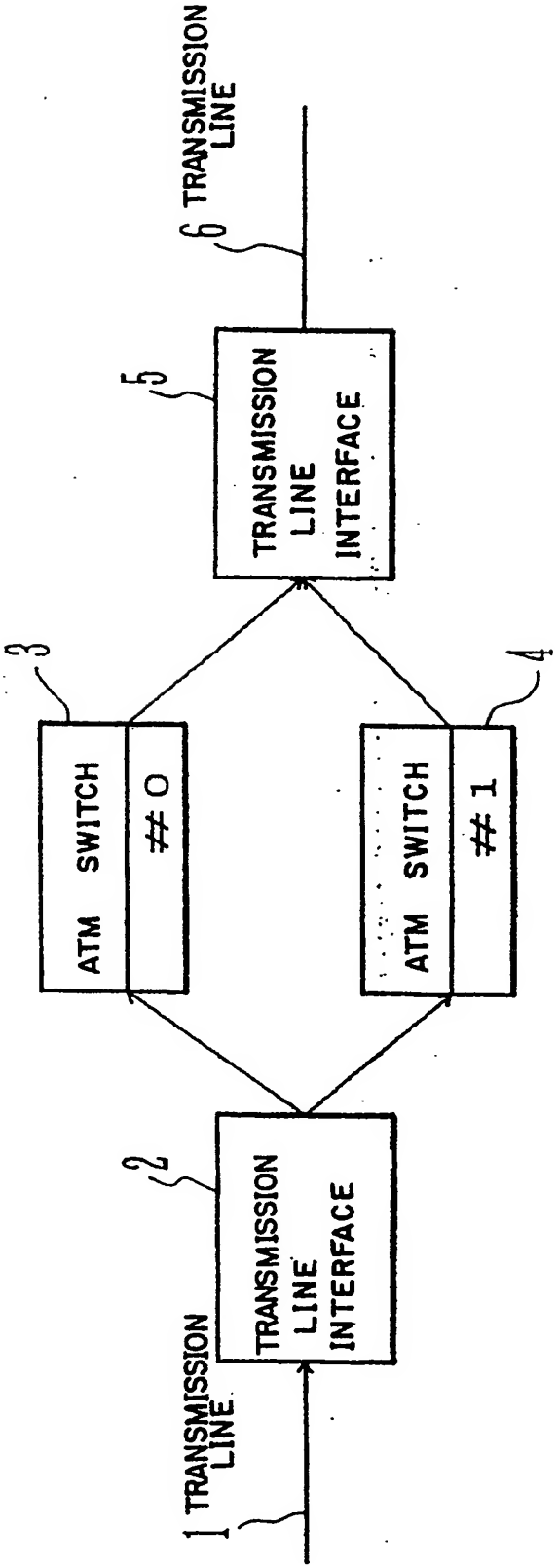
1 TRANSMISSION LINE
2
TRANSMISSION LINE INTERFACE
3
ATM SWITCH #0
4
ATM SWITCH #1
5
TRANSMISSION LINE INTERFACE
6 TRANSMISSION LINE

Fig. 2

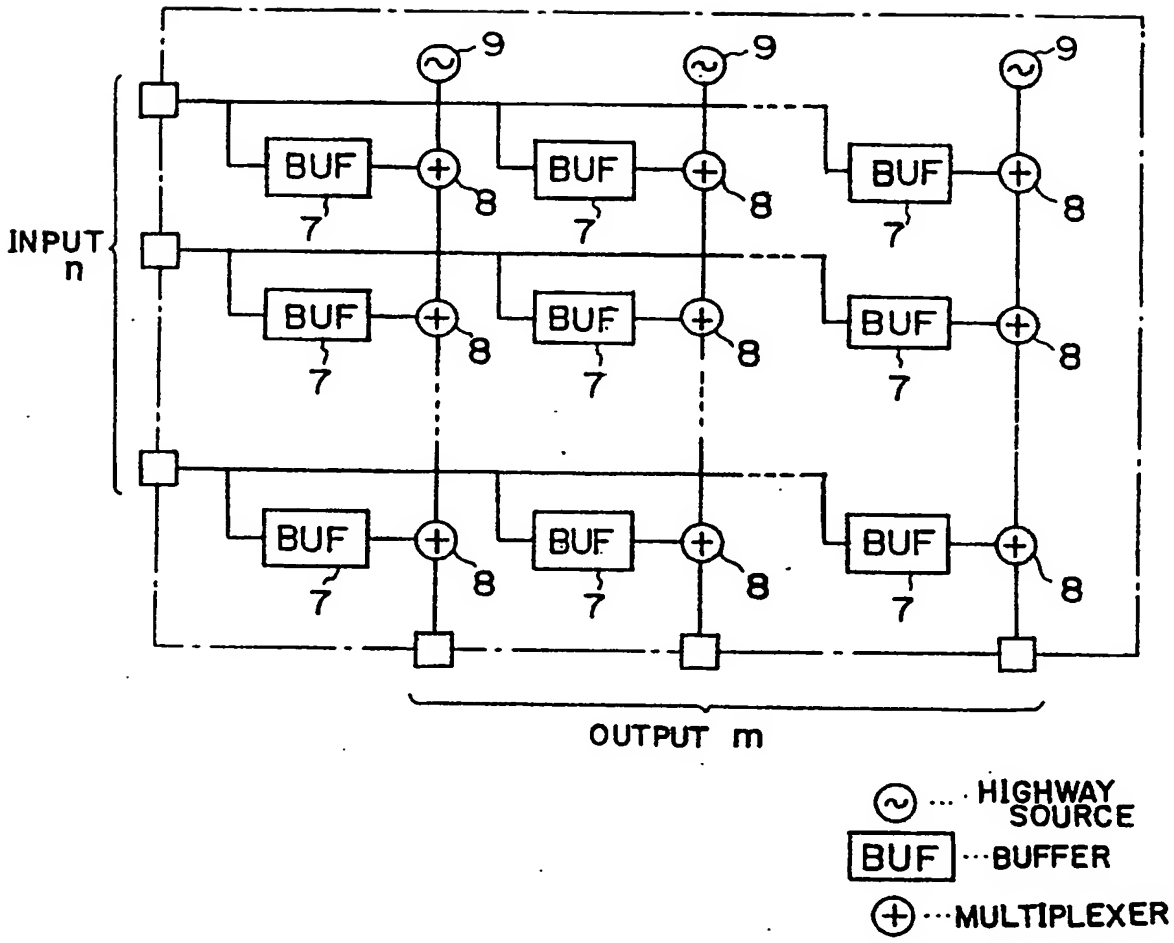
9
BUF
7
8
INPUT
n
OUTPUT m
... HIGHWAY SOURCE
BUF ... BUFFER
... MULTIPLEXER

Fig. 3

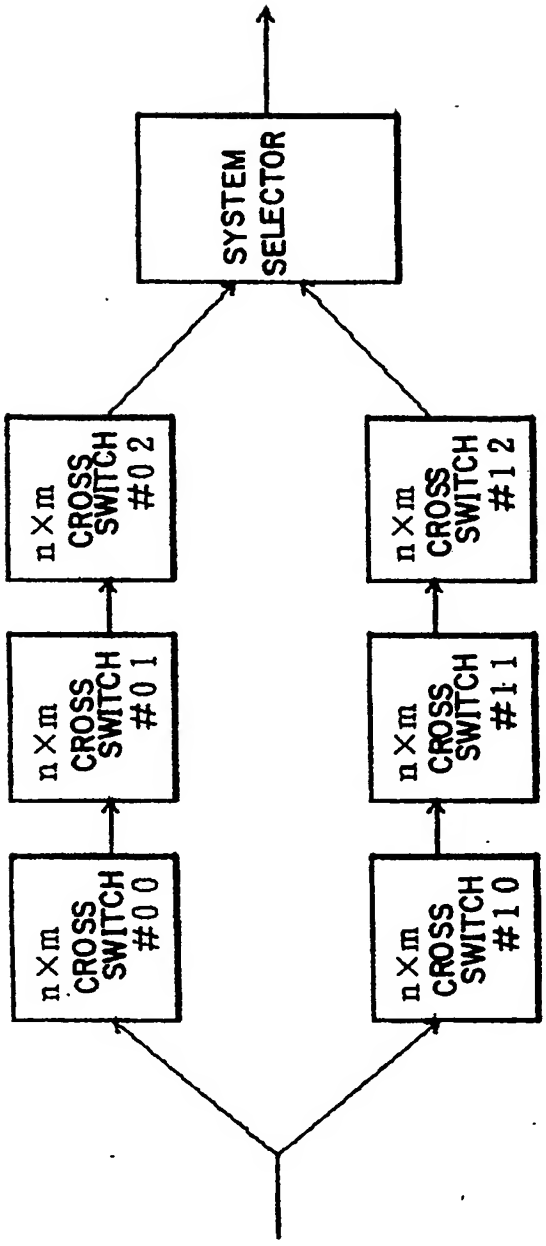
SYSTEM SELECTOR
n X m CROSS SWITCH #02
n X m CROSS SWITCH #12
n X m CROSS SWITCH #01
n X m CROSS SWITCH #11
n X m CROSS SWITCH #00
n X m CROSS SWITCH #10

Fig. 4

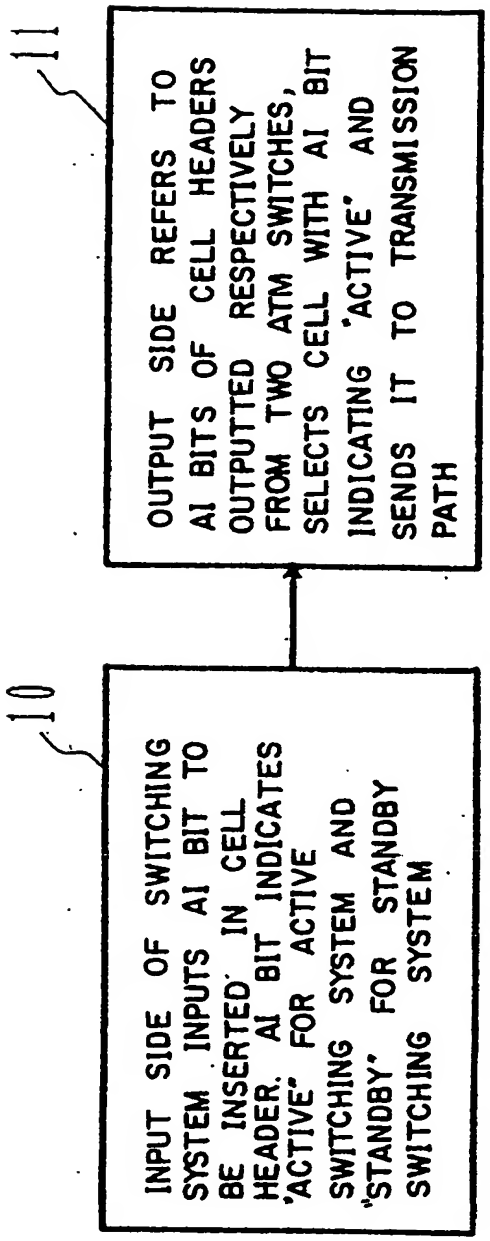
10
INPUT SIDE OF SWITCHING SYSTEM INPUTS AI BIT TO BE INSERTED IN CELL HEADER. AI BIT INDICATES 'ACTIVE' FOR ACTIVE SWITCHING SYSTEM AND 'STANDBY' FOR STANDBY SWITCHING SYSTEM
11
OUTPUT SIDE REFERS TO AI BITS OF CELL HEADERS OUTPUTTED RESPECTIVELY FROM TWO ATM SWITCHES, SELECTS CELL WITH AI BIT INDICATING 'ACTIVE' AND SENDS IT TO TRANSMISSION PATH

Fig. 5

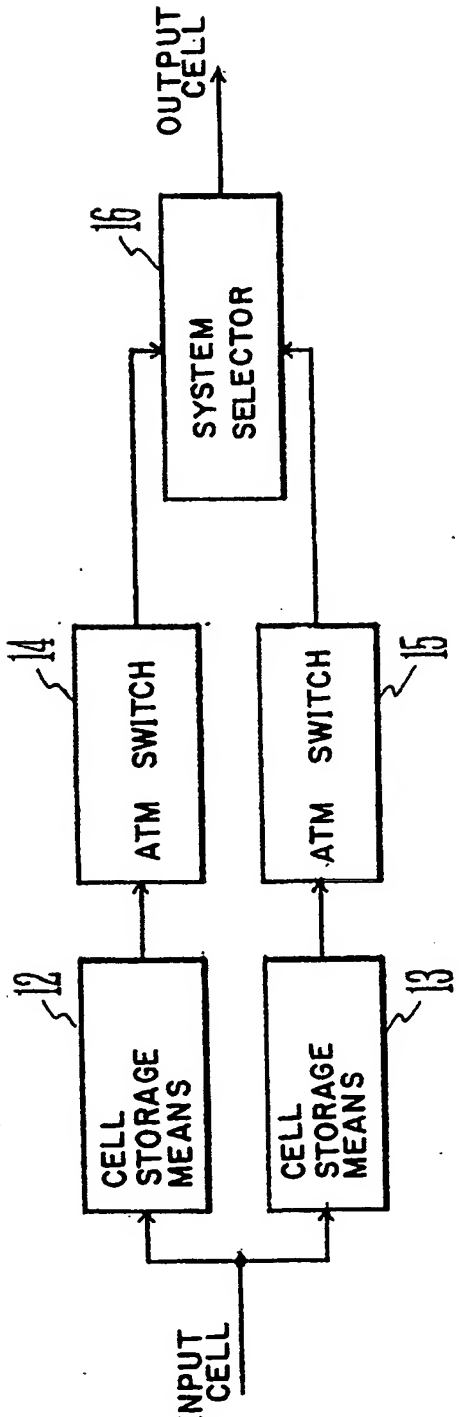
OUTPUT CELL
16
SYSTEM SELECTOR
14
ATM SWITCH
15
ATM SWITCH
12
CELL STORAGE MEANS
13
CELL STORAGE MEANS
INPUT CELL

Fig. 6

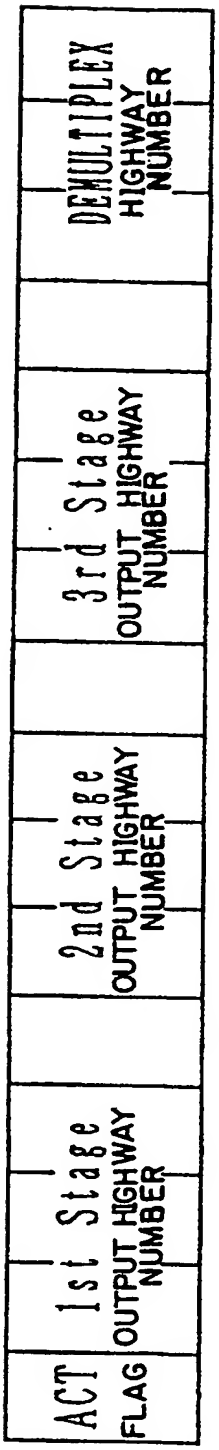
ACT FLAG
1st Stage OUTPUT HIGHWAY NUMBER
2nd Stage OUTPUT HIGHWAY NUMBER
3rd Stage OUTPUT HIGHWAY NUMBER
DEMULTIPLEX HIGHWAY NUMBER

Fig. 7

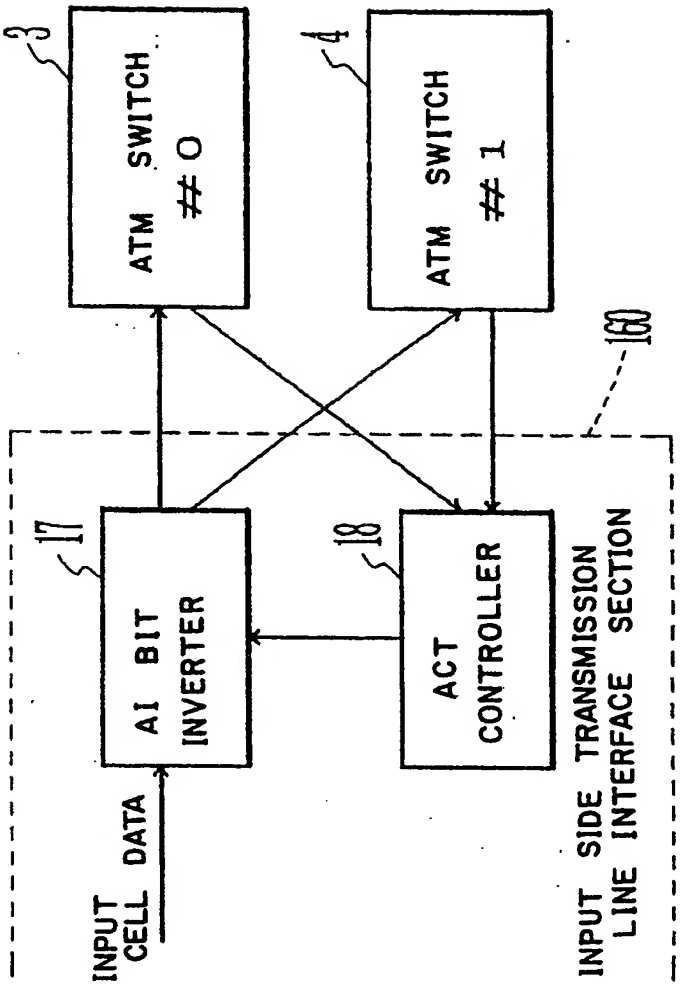
3
ATM SWITCH #0
4
ATM SWITCH #1
160
17
AI BIT INVERTER
18
ACT CONTROLLER
INPUT CELL DATA
INPUT SIDE TRANSMISSION LINE INTERFACE SECTION

Fig. 8

ATM SWITCH #0	ATM SWITCH #1	ACT CONTROLLER GENERATION INFORMATION
ACT	ACT	HOLD PREVIOUS STATE
ACT	ACT	#0 ACT #1 SBY
SBY	SBY	#0 SBY #1 ACT
SBY	SBY	HOLD PREVIOUS STATE

Fig. 9

EP 0 455 827 A1

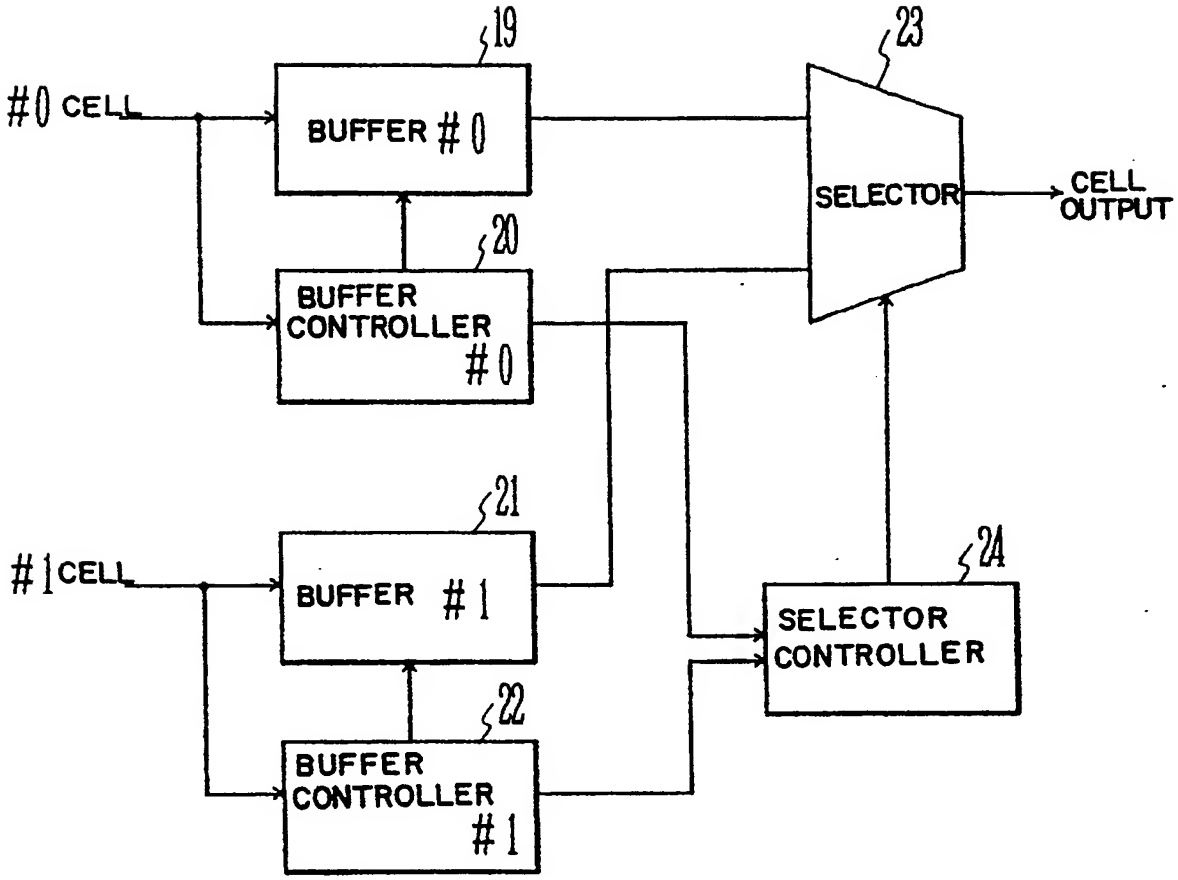
#0 CELL
19
BUFFER #0
23
SELECTOR
CELL OUTPUT
20
BUFFER CONTROLLER #0
#1 CELL
21
BUFFER #1
24
SELECTOR CONTROLLER
22
BUFFER CONTROLLER #1

Fig. 10

BUFFER #0	BUFFER #1	SELECTOR CONTROL
EMPTY	EMPTY	PREVIOUS STATE
EMPTY	HAVE DATA	FROM BUFFER # 1
HAVE DATA	EMPTY	FROM BUFFER # 0
HAVE DATA	HAVE DATA	PREVIOUS STATE

Fig. 11

0 SYSTEM	1 SYSTEM	SELECTION STATE
ACT	ACT	HOLD PREVIOUS STATE
ACT	SBY	0 SYSTEM
SBY	ACT	1 SYSTEM
SBY	SBY	HOLD PREVIOUS STATE

Fig. 18

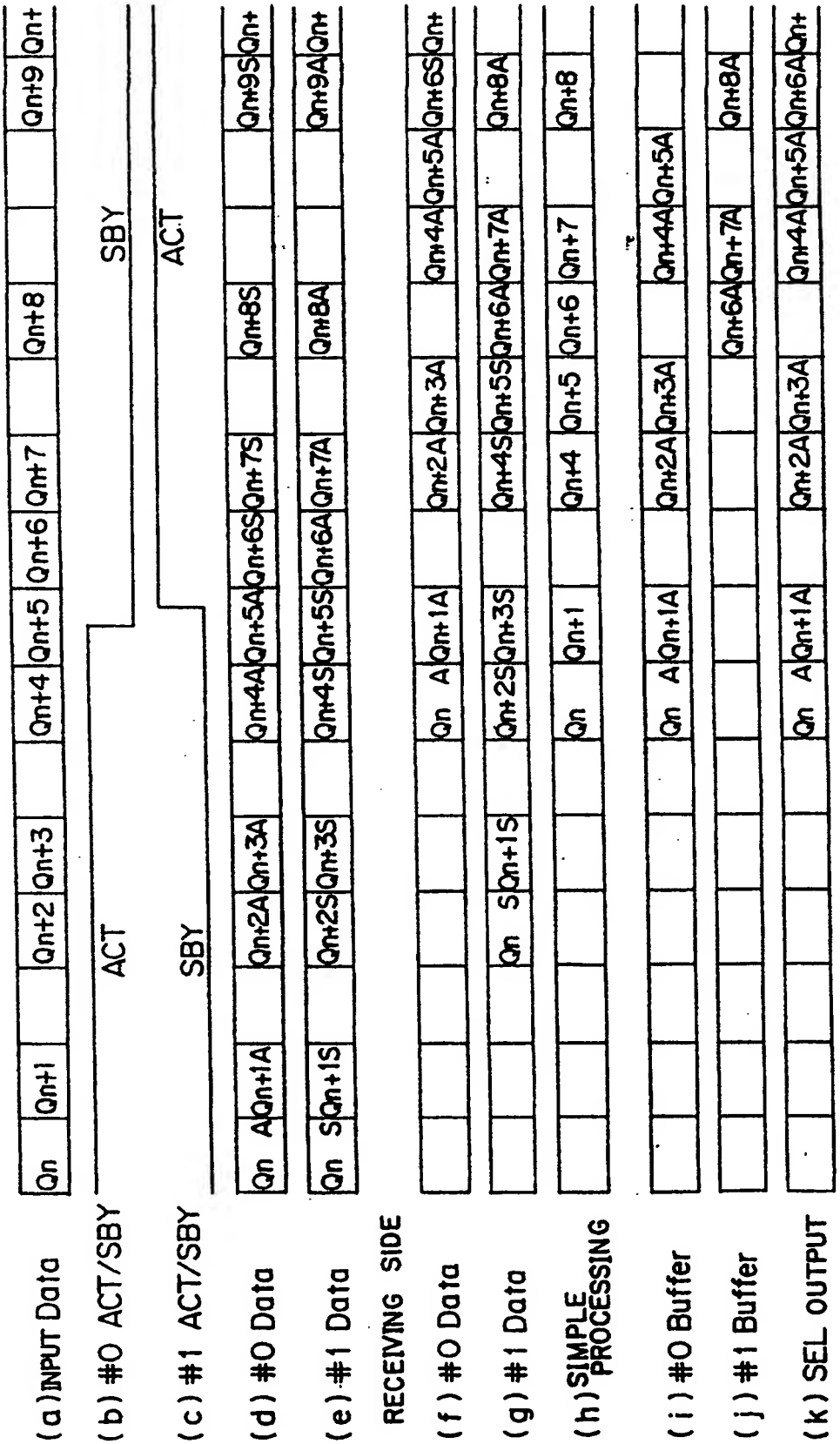
(a) INPUT Data
Qn
Qn+1
Qn+2
Qn+3
Qn+4
Qn+5
Qn+6
Qn+7
Qn+8
Qn+9
Qn+
(b) #0 ACT/SBY
ACT
SBY
(c) #1 ACT/SBY
SBY
ACT
(d) #0 Data
Qn A
Qn+1A
Qn+2A
Qn+3A
Qn+4A
Qn+5A
Qn+6S
Qn+7S
Qn+8S
Qn+9S
Qn+
(e) #1 Data
Qn S
Qn+1S
Qn+2S
Qn+3S
Qn+4S
Qn+5S
Qn+6A
Qn+7A
Qn+8A
Qn+9A
Qn+
RECEIVING SIDE
(f) #0 Data
Qn A
Qn+1A
Qn+2A
Qn+3A
Qn+4A
Qn+5A
Qn+6S
Qn+
(g) #1 Data
Qn S
Qn+1S
Qn+2S
Qn+3S
Qn+4S
Qn+5S
Qn+6A
Qn+7A
Qn+8A
(h) SIMPLE PROCESSING
Qn
Qn+1
Qn+4
Qn+5
Qn+6
Qn+7
Qn+8
(i) #0 Buffer
Qn A
Qn+1A
Qn+2A
Qn+3A
Qn+4A
Qn+5A
(j) #1 Buffer
Qn+6A
Qn+7A
Qn+8A
(k) SEL OUTPUT
Qn A
Qn+1A
Qn+2A
Qn+3A
Qn+4A
Qn+5A
Qn+6A
Qn+

Fig. 12

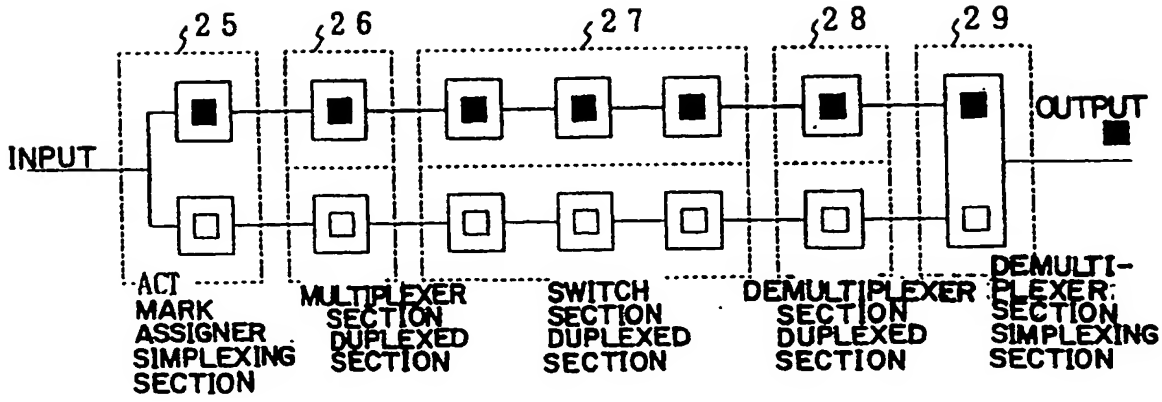
25
26
27
28
29
INPUT
OUTPUT
ACT MARK ASSIGNER SIMPLEXING SECTION
MULTIPLEXER SECTION DUPLEXED SECTION
SWITCH SECTION DUPLEXED SECTION
DEMULTIPLEXER SECTION DUPLEXED SECTION
DEMULTI-PLEXER SECTION SIMPLEXING SECTION

Fig. 13

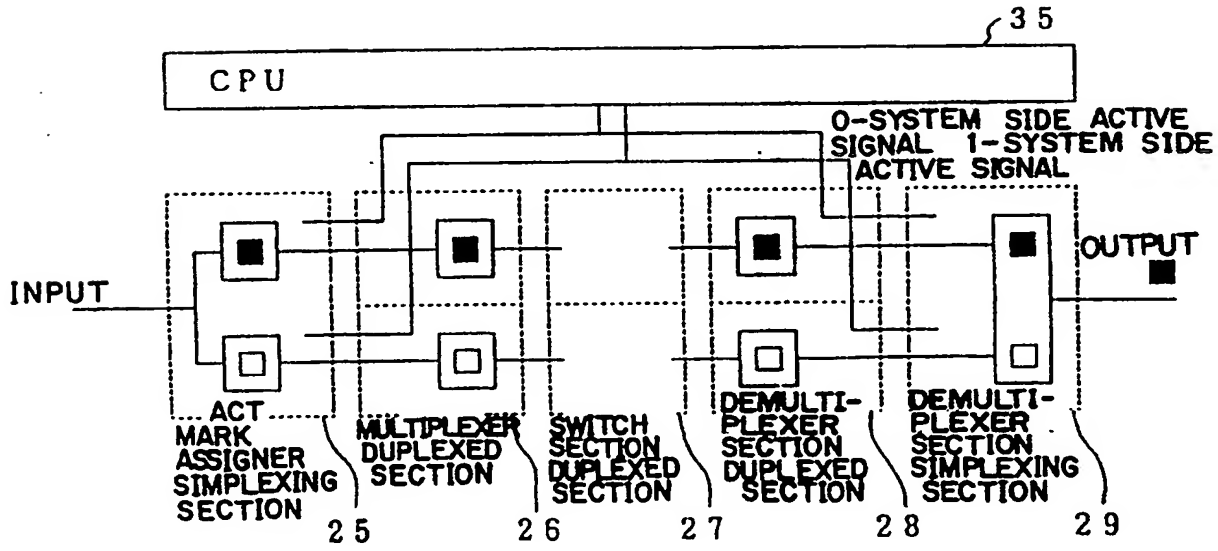
35
CPU
0-SYSTEM SIDE ACTIVE SIGNAL
1-SYSTEM SIDE ACTIVE SIGNAL
INPUT
OUTPUT
ACT MARK ASSIGNER SIMPLEXING SECTION
MULTIPLEXER DUPLEXED SECTION
SWITCH SECTION DUPLEXED SECTION
DEMULTI-PLEXER SECTION DUPLEXED SECTION
DEMULTI-PLEXER SECTION SIMPLEXING SECTION
25
26
27
28
29

Fig. 17

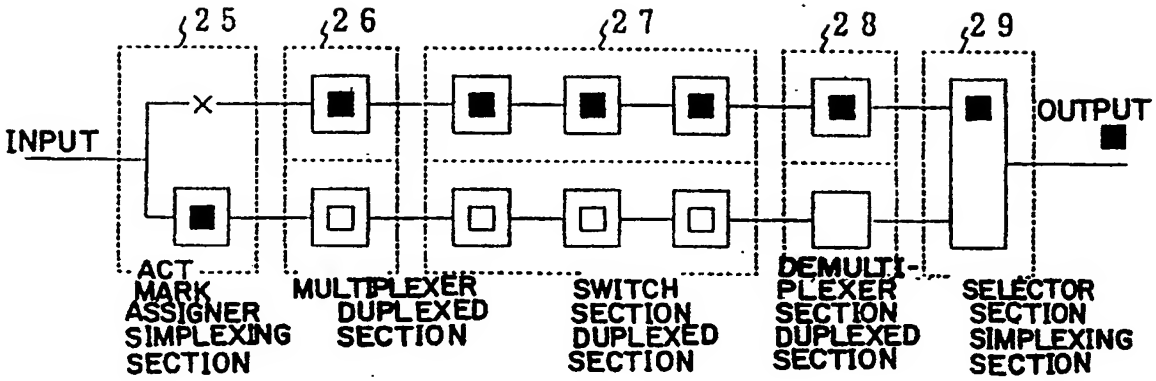

Fig. 14 (a)

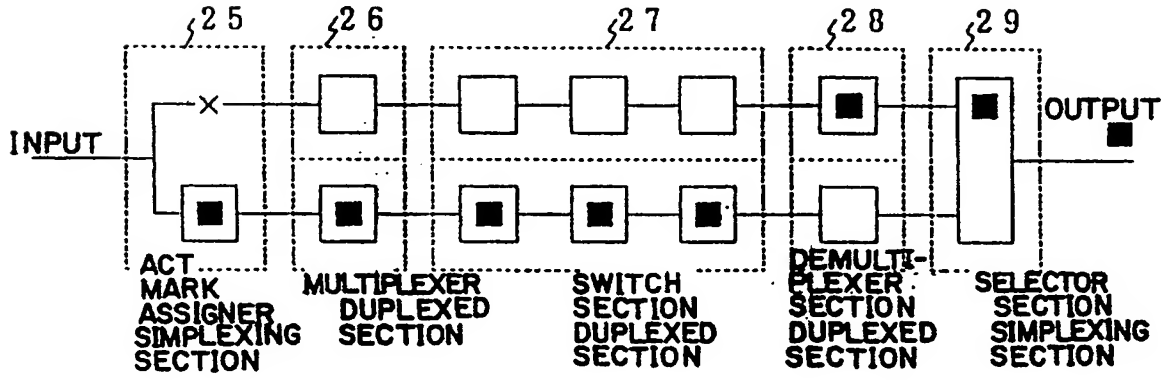

Fig. 14 (b)

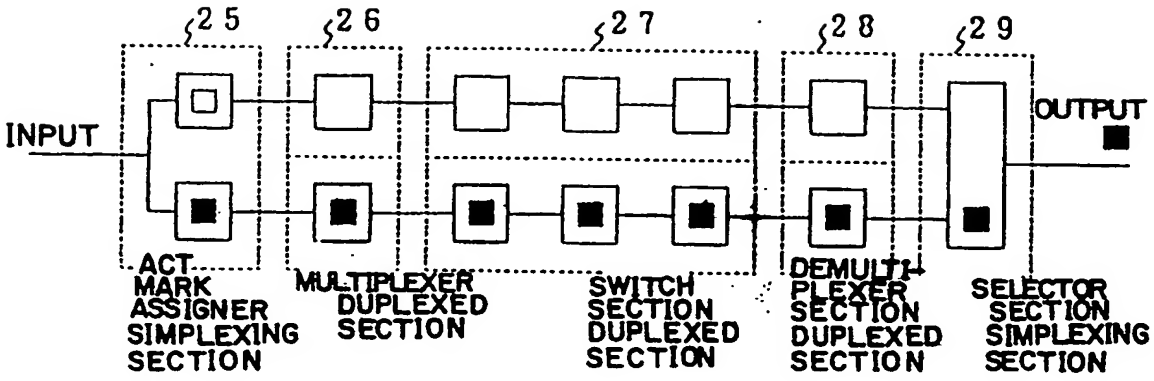

Fig. 14 (d)

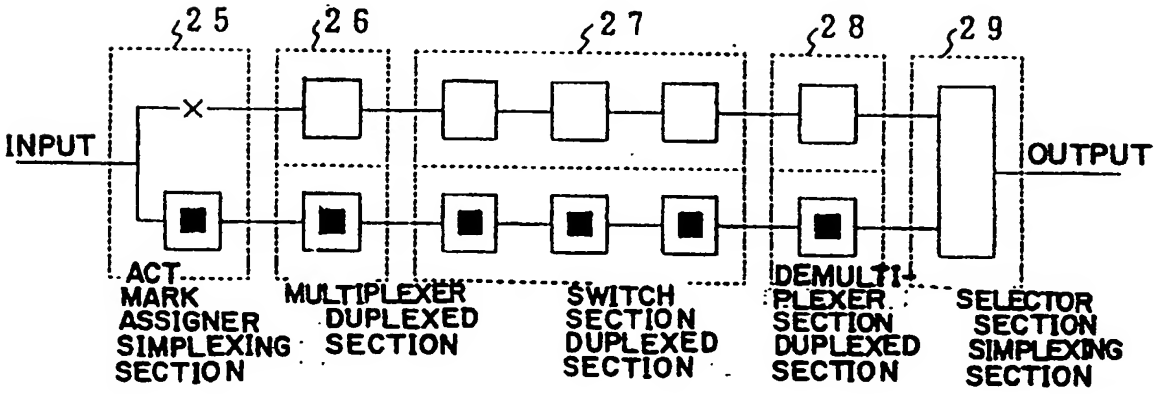

Fig. 14 (c)

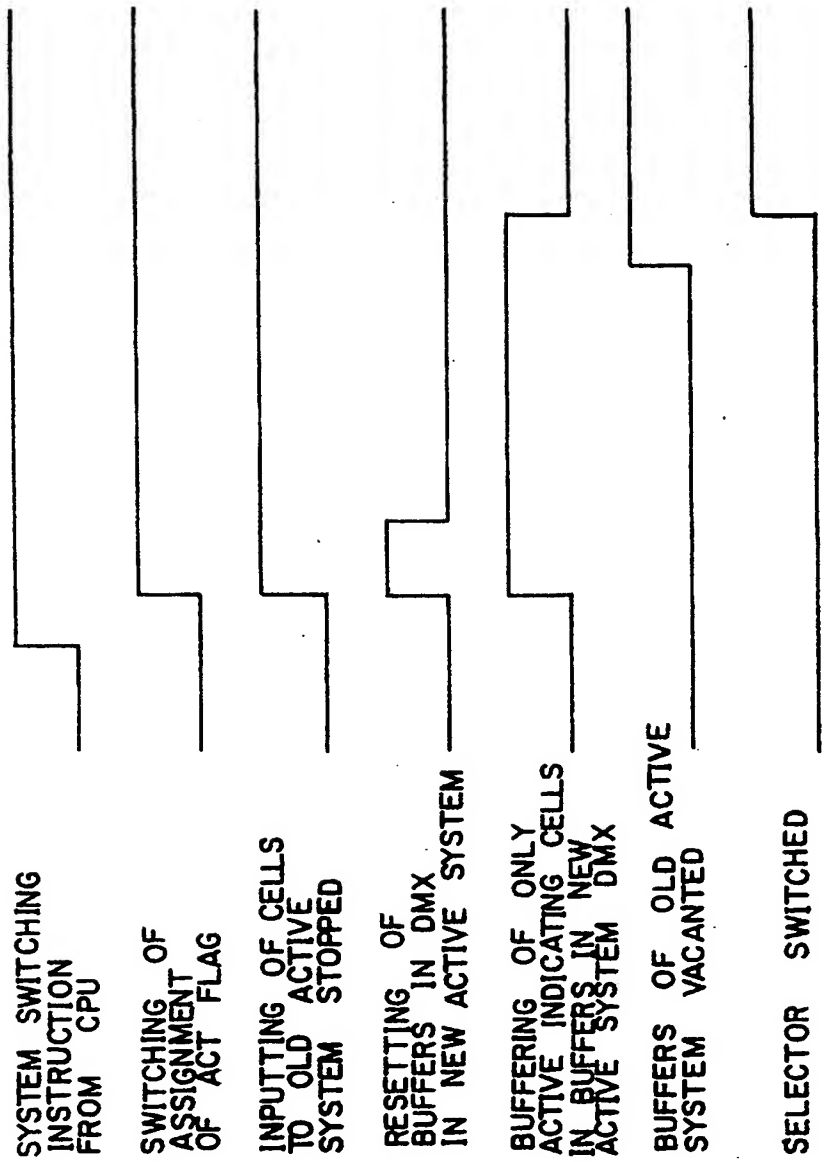
SYSTEM SWITCHING INSTRUCTION FROM CPU
SWITCHING OF ASSIGNMENT OF ACT FLAG
INPUTTING OF CELLS TO OLD ACTIVE SYSTEM STOPPED
RESETTING OF BUFFERS IN DMX IN NEW ACTIVE SYSTEM
BUFFERING OF ONLY ACTIVE INDICATING CELLS IN BUFFERS IN NEW ACTIVE SYSTEM DMX
BUFFERS OF OLD ACTIVE SYSTEM VACANTED
SELECTOR SWITCHED

Fig. 15

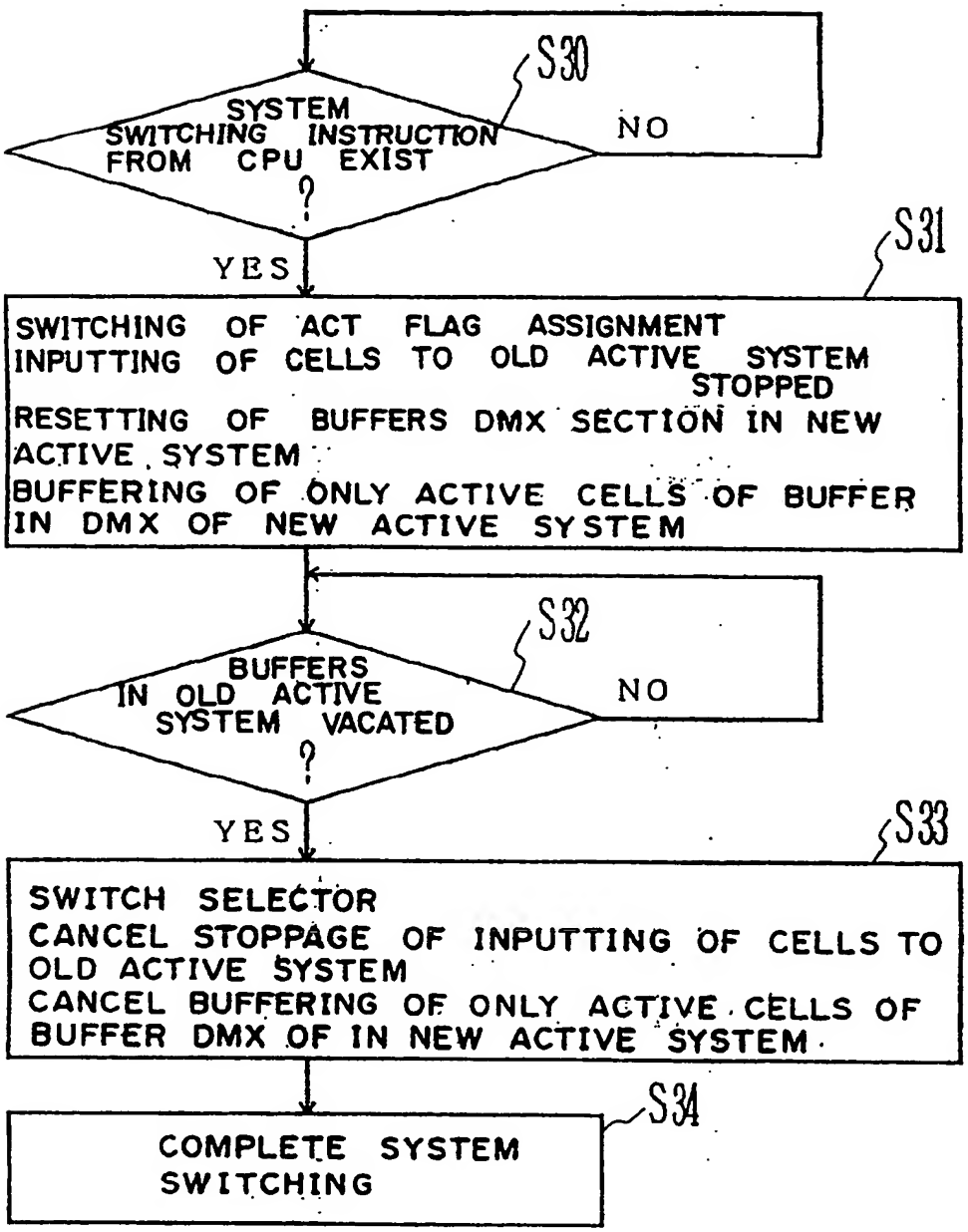
S30
SYSTEM SWITCHING INSTRUCTION FROM CPU EXIST ?
NO
YES
S31
SWITCHING OF ACT FLAG ASSIGNMENT
INPUTTING OF CELLS TO OLD ACTIVE SYSTEM STOPPED
RESETTING OF BUFFERS DMX SECTION IN NEW ACTIVE SYSTEM
BUFFERING OF ONLY ACTIVE CELLS OF BUFFER IN DMX OF NEW ACTIVE SYSTEM
S32
BUFFERS IN OLD ACTIVE SYSTEM VACATED ?
NO
YES
S33
SWITCH SELECTOR
CANCEL STOPPAGE OF INPUTTING OF CELLS TO OLD ACTIVE SYSTEM
CANCEL BUFFERING OF ONLY ACTIVE CELLS OF BUFFER DMX OF IN NEW ACTIVE SYSTEM
S34
COMPLETE SYSTEM SWITCHING

Fig. 16

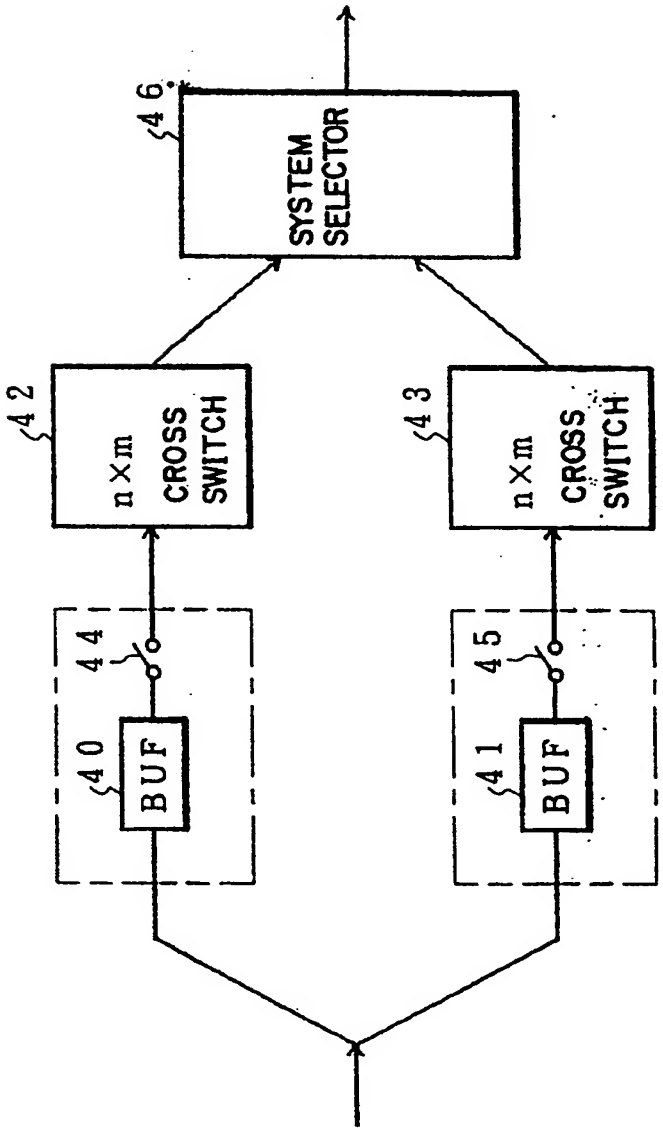
46
SYSTEM SELECTOR
42
n×m CROSS SWITCH
43
n×m CROSS SWITCH
44
45
40
BUF
41
BUF

Fig. 19

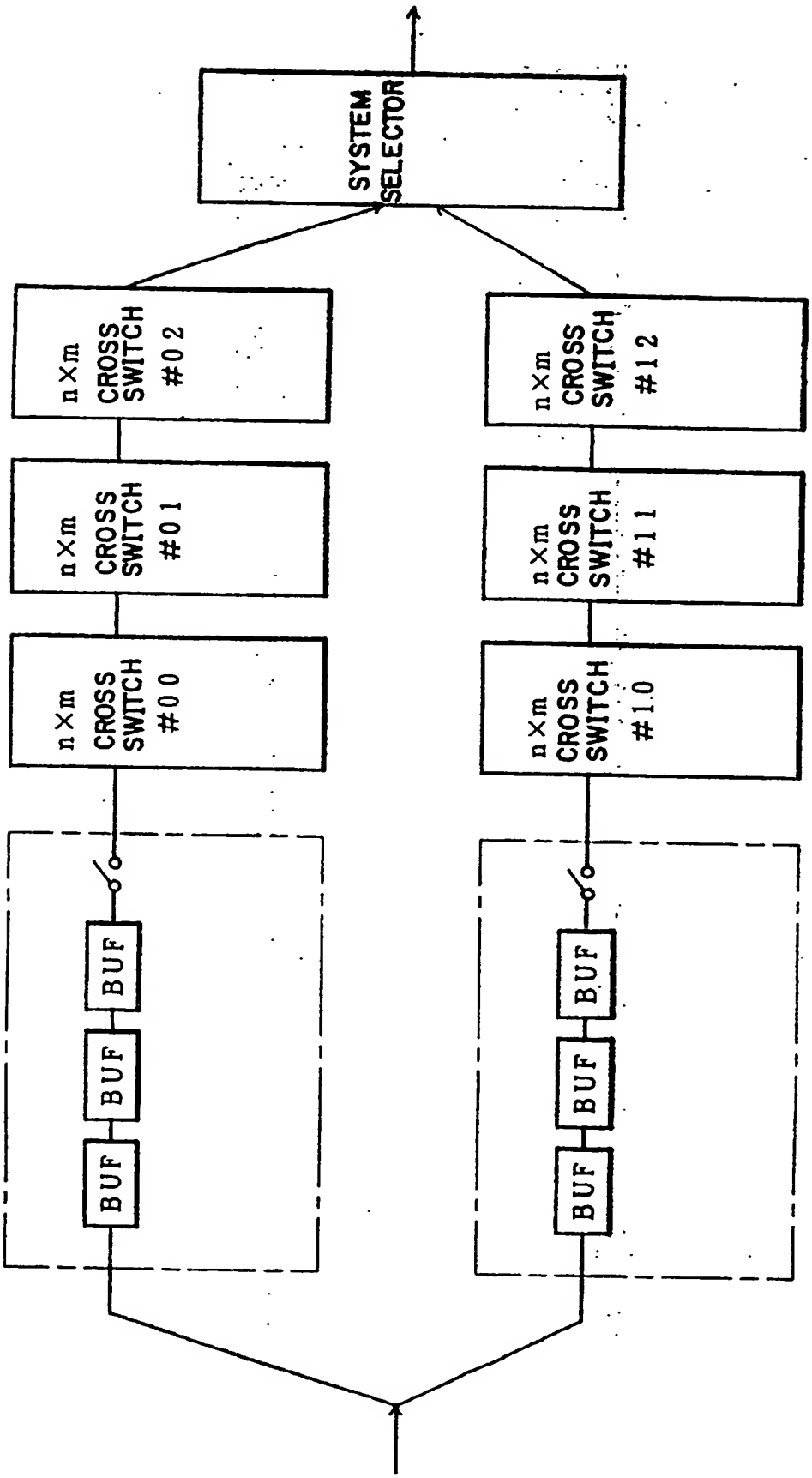
SYSTEM SELECTOR
n×m CROSS SWITCH #02
n×m CROSS SWITCH #12
n×m CROSS SWITCH #01
n×m CROSS SWITCH #11
n×m CROSS SWITCH #00
n×m CROSS SWITCH #10
BUF
BUF
BUF
BUF
BUF
BUF

Fig. 20

INTERNATIONAL SEARCH REPORT

International Application No PCT/JP90/01556

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl[5] H04L12/48

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC	H04L12/48, 29/14

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

Jitsuyo Shinan Koho	1926 - 1990
Kokai Jitsuyo Shinan Koho	1971 - 1990

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	JP, A, 1-292936 (Hitachi, Ltd.), November 27, 1989 (27. 11. 89), Lines 1 to 10, lower right column, page 2, Fig. 3 (Family: none)	10
Y	JP, A, 63-232659 (Fujitsu Ltd.), September 28, 1988 (28. 09. 88), Claim, Figs. 2, 3 (Family: none)	10

* Special categories of cited documents: [10]

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"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
February 5, 1991 (05. 02. 91)	February 18, 1991 (18. 02. 91)
International Searching Authority	**Signature of Authorized Officer**
Japanese Patent Office	

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